METHOD AND/OR CIRCUIT FOR IMPLEMENTING A ZOOM IN A VIDEO SIGNAL

Field of the Invention

The present invention relates to video signals generally and, more particularly, to a method and/or circuit for implementing a zoom in a video signal.

Background of the Invention

Conventional solutions for implementing a zoom feature in a video system use extra hardware in addition to the hardware needed to generate and process the video. The extra hardware is dedicated to implementing the zoom. Implementing extra hardware adds to the overall cost of a system. Also, conventional zooms are typically available for playback only (i.e., not available on echo during record). Conventional zoom features do not provide a high quality zoom (i.e., with a minimum of artifacts), particularly when implemented in interlaced video.

It would be desirable to implement a zoom feature that minimizes artifacts and may be implemented by incorporating existing hardware.

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Summary of the Invention

One aspect of the present invention concerns an apparatus comprising a de-interlacer circuit, a rate converter circuit and a zoom circuit. The de-interlacer circuit may be configured to

5   generate a first progressive signal having a first rate in response to an interlaced signal. The rate converter circuit may be configured to generate a second progressive signal having a second rate in response to the first progressive signal. The zoom circuit may be configured to generate an output video signal in response to

10   the second progressive signal. The output video signal may represent a portion of the second progressive signal having a frame size equal to a frame size of the interlaced signal.

Another aspect of the present invention concerns a method for implementing a zoom in a digital video signal comprising the

15   steps of (A) converting an interlaced video signal to a first progressive video signal having a first rate, (B) generating a second video signal having a second rate in response to the first video signal and (C) generating an output video signal in response to the second video signal. The output video signal may represent

20   a portion of the second video signal having a frame size equal to a frame size of the interlaced signal.

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The objects, features and advantages of the present invention include implementing method and/or circuit for providing a zoom in a video system that may (i) provide better picture quality than a conventional zoom, (ii) provide a zoom feature on

5   either playback or on an echo during record, (iii) provide better picture quality for both film and video content, (iv) provide better picture quality for zoom during video format conversion, and/or (v) provide simplicity for incorporation into future processor generations by scaling the design.

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Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

15   FIG. 1 is a diagram of a zoom implementation;

FIG. 2 is another diagram of a zoom implementation;

FIG. 3 is a diagram illustrating a zoom transformation;

FIG. 4 is a diagram illustrating an example of an implementation of field filtering for a 2x vertical zoom is shown;

20   FIG. 5 is a diagram illustrating an implementation of frame filtering for a 2x vertical zoom is shown; and

FIG. 6 is a block diagram illustrating an example of progressive dropping before re-interlacing.

Detailed Description of the Preferred Embodiments

5   The present invention may be implemented to reduce the complexity of implementing a zoom feature.   A hardware implementation may be used that supports future generation processors (e.g., the Domino processor, available from LSI Logic of Milpitas, California).   The present invention may enhance the

10   picture quality of a zoom by providing a video image free from digital artifacts.   The present invention may be used for either (i) playback or (ii) as an echo during record.

A zoom is a popular feature in DVD players/recorders and television set-top boxes (STB).   The present invention may

15   implement a zoom based on True Scan Pro technology, available from LSI Logic of Milpitas, California.   This method simplifies the implementation of such a feature and greatly reduces the chance of common artifacts like combing noise.

Referring to FIG. 1, a circuit 100 is shown implementing

20   an audio/video presentation system.   The circuit 100 generally comprises a video frame rate converter block (or circuit) 102, an

audio and video synchronization block (or circuit) 104, a zoom

block (or circuit) 105, an interlaced to progressive block (or

circuit) 106, a video presentation block (or circuit) 108 and an

audio presentation block (or circuit) 110. The zoom block

5   generally comprises a horizontal zoom block (or circuit) 120, a

field frame decision block (or circuit) 122, a vertical field zoom

block (or circuit) 124 and a vertical frame zoom block (or circuit)

126. The field/frame decision block 122 selects either the

vertical field zoom block 124 or the vertical frame zoom block 126.

10   Referring to FIG. 2, a circuit 200 is shown illustrating

a zoom system. The circuit 200 generally comprises an interlaced

to progressive conversion block (or circuit) 202, a video frame

rate converter block (or circuit) 204, an audio and video

synchronization block (or circuit) 206, a zoom block (or circuit)

15   207, a re-interlacer block (or circuit) 208, a video presentation

block (or circuit) 210, and an audio presentation block (or

circuit) 212. The zoom circuit 207 generally comprises a

horizontal zoom block (or circuit) 220 and a vertical zoom block

(or circuit) 222. The re-interlacer circuit 208 may be used if an

20   interlaced signal is desirable for a particular display device.

However, the re-interlacer circuit 208 may not be needed in all

design implementations. The video presentation circuit 210 may be a video monitor or other display device. The audio presentation circuit 212 may be implemented as a speaker or other device.

The interlaced to progressive circuit 202 may be implemented as a True Scan Pro technology, available from LSI Logic, Milpitas, California. However, other circuits that convert an interlaced signal to a progressive signal may be implemented to meet the design criteria of a particular implementation. The video frame rate converter circuit 204 may be implemented to operate in the progressive domain. The video frame rate converter circuit 204 may repeat or drop a frame based on the timestamp of the incoming frames and the selected video output frame rate. The video frame rate converter circuit 204 may also vertically resizing each frame to the desired output format (e.g., 480 input lines from NTSC source material may be resized to 576 output lines for PAL format display or vice-versa).

The audio and video synchronization circuit 206 may be used to synchronize video and audio samples to a common clock to ensure "lip-sync" during the presentation. The zoom circuit 208 may be implemented to extract a portion of the input frame to expand to a full-screen output size. The zoom circuit 208

processes an input signal that is in a progressive format (e.g., 60 frames per second).

The re-interlacer circuit 210 may be an optional circuit that may convert back to an interlaced format (e.g., NTSC or PAL).

5   The re-interlacer circuit 210 may extract half the lines of each input frame, typically used in all TV scanning equipment. While modern video displays normally accept a progressive signal, older displays may still need an interlaced signal. Furthermore, video scalers often use an interlaced signal rather than a progressive

10   signal.

Referring to FIG. 3, an example of a zoom transformation is shown. An input picture 230 is shown having a region 232. The region 232 needs to be expanded to fit the output picture 234. The output picture 234 is created by vertically and horizontally

15   filtering the region 232. Extra care needs to be taken when performing vertical filtering, since the picture 230 is made of 2 independent fields. In particular, a video frame is made of two distinct video fields that are presented at different times (e.g., $1/50^{th}$ of a second apart in video formats like PAL, $1/60^{th}$ of a

20   second apart in video formats like NTSC).

Several different processes may have created the content of the video frame. A first process (or case) may be a video camera (e.g., sampling interlaced fields at the field rate, creating video fields the same way as taking a picture every 1/50th

5   or 1/60th of a second depending on the video format). A second process (or case) may be the telecine machine converting 24 frame-per-second movies into video, or 12 frame-per-second cartoons in video for example.

In the first case, the two video fields have been sampled

10   at different times and need to be presented with the correct delay between then. In the second case, some video fields may just be sampled at the same time, presenting a still image. One field may be the top lines. The other field may be the bottom lines (interlaced) of the same image. Not all of the fields may be

15   sampled.

In the first case, vertical filtering may be implemented on a field by field base (called field filtering). Field filtering normally avoids having one field "bleed" into the other and vice versa. Field filtering avoids the so-called "combing" noise in the

20   resulting picture. In the second case, vertical filtering may be implemented on the whole frame (called frame filtering), rather

than field-by-field, creating a picture with better definition (or less blurriness). The vertical zoom circuit 222 is generally implemented as frame filtering. There are no such field/frame distinctions in the horizontal filtering.

5   The present invention is generally based on progressive input frames and generally relies on using frame-based only vertical filtering. Simple frame-based vertical filtering avoids complex process decisions and can easily be implemented in hardware (VLSI) for a cost effective solution. Since the present invention

10   is based on progressive input frames, visual artifacts like "combing noise" found in poor vertical filtering of interlaced video are normally avoided.

        Referring to FIG. 4, a diagram illustrating an implementation of field filtering for a 2x vertical zoom is shown.

15   The main idea of field filtering is that only odd lines of the input video frame contribute to create the odd lines of the output video frame. In the example of FIG. 4.:

        The output frame Odd1 is made from the input frame Odd1. The output frame Odd2 is made of combination of the input frame

20   Odd1 and the input frame Odd2. The output frame Odd3 is made of the input frame Odd2. The output frame Odd4 is made of combination

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of the input frame Odd2 and the input frame Odd3. The sequence

repeats for the remaining frames.

Similarly, even output lines are created only from input

even lines. Since odd and even fields are presented at different

5   times,   each   field   corresponding   to   a   different   time   stamp

(sampling).   Since odd frames and even frames are matched, each

output field is created from the respective time stamps. The time

stamps are maintained on a per field basis. Since the input frame

is a "progressive" picture (meaning that both fields are from the

10   same original picture) the field processing creates output lines

from input lines being 2 input frame lines apart (skipping over the

opposite field), losing definition in the rescaling process.

Referring   to   FIG.   5,   an   example   illustrating   an

implementation of frame filtering for a 2x vertical zoom is shown.

15   The input lines of the input video frame contribute to create each

of the lines of the output video frame.   In the example shown in

FIG. 5:

The output frame Odd1 is made from the input frame Odd1.

The output frame even1 is made of the combination of the input

20   frame Odd1 and the frame even1. The output frame Odd2 is made from

the input frame even1.   The output frame even2 is made from the

combination of the input frame even1 and the input frame Odd2. The

output frame Odd3 is made of the input frame Odd2. The output

frame even3 is made of the combination of the input frame Odd2 and

the input frame even2. The path repeats for the rest of the

5   frames.

Similarly, all output lines are created from all input

lines, regardless of the interlacing aspect since the original

picture is "progressive" (i.e., still picture which both fields

belong to the same time stamp). Since line samples creating the

10   output lines are close to each other, better definition may be

achieved. When dealing with video material (fields belonging to

different time stamps) since combining odd and even fields to

create output lines creates the so-called "combing-noise" effect

when such fields correspond to different time samples. The

15   vertical zoom circuit 222 normally implements the filtering shown

in FIG. 5.

Referring to FIG. 6, an example of a system 260

illustrating a zoom on a progressive signal is shown. The system

comprises the conversion circuit 202, the frame rate conversion

20   circuit 204, a vertical rescaling circuit 240, a zoom circuit 242

and the re-interlace circuit 208. By using the de-interlacing

circuit 202, a progressive video signal (e.g., V2) is created in response to an interlaced video signal (e.g., V1). By converting to the progressive signal V2 before further processing and/or conversion, the concept of top/bottom fields is not relevant for

5   additional processing. Rather, the progressive frames of the signal V2 are each positioned at a field-time interval (e.g., every $1/60^{th}$ of a second). A frame rate conversion circuit 204 drops one progressive frame every six input frames, creating a progressive output signal (e.g., V3) at the desired rate (e.g., 50Hz), with

10   smooth motion. Each output frame of the signal V3 is progressive (e.g., having 525 lines operating at 50Hz). The vertical rescaler 240 generates a signal (e.g., V4) having, for example, 625 lines operating at 50Hz. The zoom circuit 242 generates a signal (e.g., V5) having, for example, 525 lines operating at 50Hz.

15   The vertical rescaler circuit 240 only needs to perform progressive or frame-based filtering to adjust the size and does not need to perform complex field/frame decisions. The re-interlacer circuit 208 generates a signal (e.g., V6) having, for example, 625 lines operating at 25Hz. The re-interlacer circuit

20   208 extracts the top or bottom lines of each incoming frame to create an interlaced result in a format presentable by an

interlaced video display. The particular resolutions (e.g., 525 lines, 625 lines, etc.) and the particular operating frequencies (e.g., 25Hz, 30Hz, 50Hz, 60Hz, etc.) may be modified to meet the design criteria of a particular implementation.

5   While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.